Liquid Cooling

Utilizing Stacked Microchannels

Moore's Law, which states that the numbers of transistors that can be placed inexpensively on an integrated circuit will double every 18 months, has been valid for more than 50 years. But, as the transistor's size keeps shrinking, it is more difficult to put more transistors together and maintain their physical properties and electric functions. Also, it is more difficult to transfer the heat out of transistors and keep their junction temperature low. To extend Moore's Law to the foreseeable future, it will require a change from mere transistor scaling to novel packaging architectures such as so-called 3D integration, the vertical integration of chips and innovative cooling solutions.

In 2010, IBM, École Polytechnique Fédérale de Lausanne (EPFL) and the Swiss Federal Institute of Technology Zurich (ETH), signed a four-year collaborative project called CMOSAIC to understand how the latest chip cooling techniques can support a 3D chip architecture. Unlike current processors, the CMOSAIC project considers a 3D stack-architecture of multiple cores with an interconnect density from 100 to 10,000 connections per millimeter square. Researchers believe that these tiny connections and the use of hair-thin, liquid cooling microchannels, measuring only 50 microns in diameter between the active chips, are the missing links to achieving high- performance computing with future 3D chip stacks.

"In the United States, data centers already consume two percent of the electricity available, with consumption doubling every five years. In theory, at this rate, a supercomputer in the year 2050 will require the entire production of the United States' energy grid," said Prof. John R. Thome, professor of heat and mass transfer at EPFL and CMOSAIC project coordinator. 3D chip stacks with interlayer cooling not only yield higher-performance, but more importantly, allow systems with a much higher efficiency, thereby avoiding the situation where supercomputers consume too much energy to be affordable, [1]. "As we will demonstrate with ETH in the Aquasar project, employing microchannels carrying liquid coolants offers a significant advantage in addressing heat-removal challenges, and this should lead to practical 3D systems," said Bruno Michel, manager advanced thermal packaging, IBM Research - Zurich. "Water as a coolant has the ability to capture heat about 4,000 times more efficiently than air, and its heat-transporting properties are also far superior."

As the chip design goes to 3D, there comes the requirement for a cooling solution that goes three dimensions, too. Integrating a multilayer of liquid cooling microchannels inside a 3D chip structure, or using stacked microchannel heat sinks to cool high power chips, not only requires advanced micro-manufacture technology, but also relies on a fundamental understanding of the flow inside microchannels and heat transfer coupling between different layers of microchannels. This paper summarizes some recent experimental research works on stacked microchannel heat sinks by Wei [2] and Lei et al. [3].

The two-layer microchannel heat sink Wei [2] tested is illustrated in Figure 1. It consists of five layers of silicon plates. Two microchannel layers provide the cooling located at the bottom. Two manifold layers above the microchannel layers distribute the fluid. The fifth layer with inlet and outlet ports is for fluid connection. The microchannels, manifolds and inlet-outlet ports were all fabricated using the deep reactive ion etching (DRIE) technique. The dimensions of the two layers of microchannels are shown in Figure 2 and Table 1. Figure 3 shows the magnified photo of the DRIE etched microchannel heat sink.

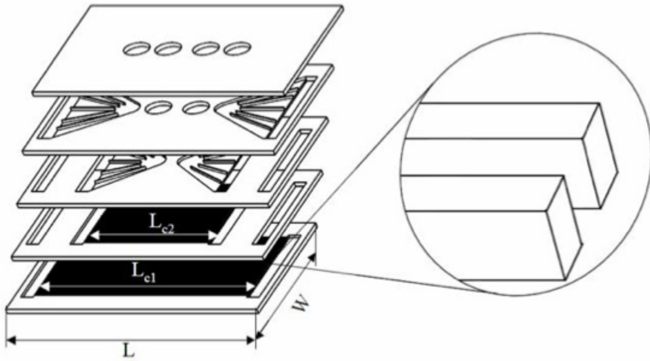

Figure 1. Two-Layer Microchannel Heat Sink Schematics [2]

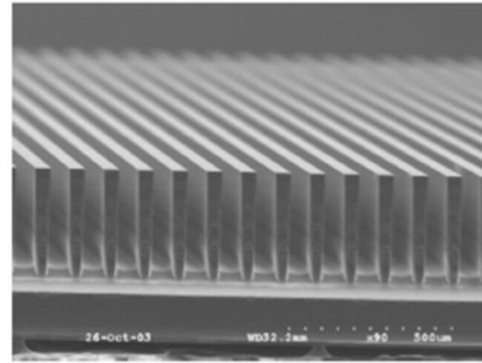

Figure 3. Photo of Magnified Microchannel Heat Sink [2]

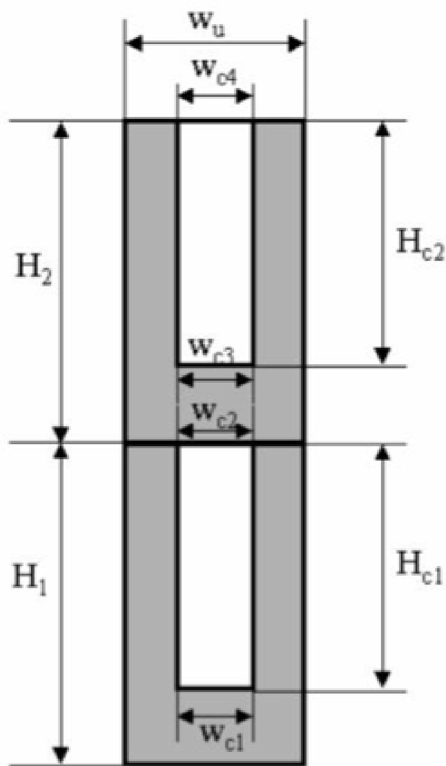

Figure 2. Two-Layer Microchannel Heat Sink Dimension [2]

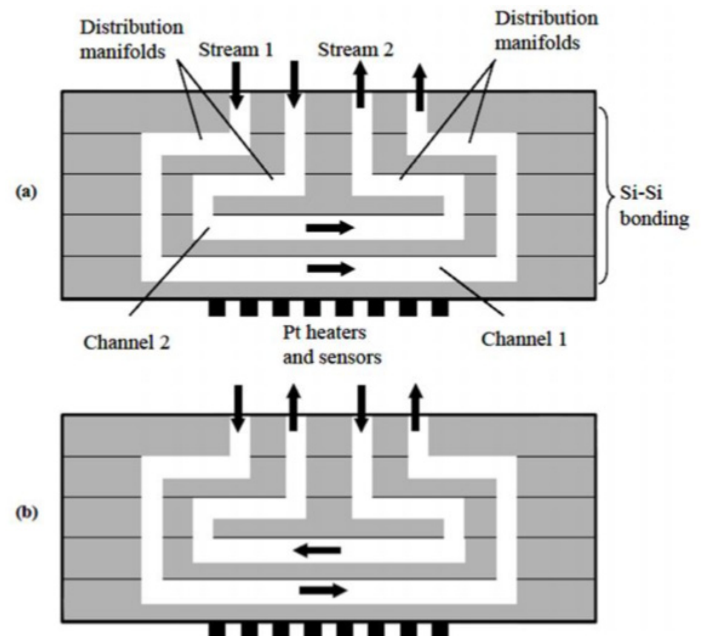

Figure 4. Schematic of Two-Layer Microchannel Heat Sink (a) Parallel Flow Arrangement (b) Counter Flow Arrangement [2]

L_{c1}	L_{c2}	W_u	W_{c1}	W_{c2}	W_{c3}
18	10	0.1	0.056	0.054	0.061
W_{c4}	H_{c1}	H_{c2}	H_1	H_2	
0.053	0.284	0.243	0.48	0.48	

Figure 1. Two-Layer Microchannel Heat Sink Schematics [2]

In Wei's [2] experiments, platinum heaters and resistive temperature sensors were deposited on the backside of the structure shown in Figure 4 to provide heating and temperature sensing respectively. The de-ionized (DI) water was used as working fluid in Wei's experiments and two different flow arrangements: parallel flow and counter flow (see Figure 4) were studied. As for the results of the experiments, Wei concludes:

1. A thermal resistance of less than 0.1 K/W was achieved for both counter flow and parallel flow configurations.
2. For the low flow rate range, the parallel flow arrangement results in a better overall thermal performance than a counter flow arrangement
3. For the large flow rate range, the thermal resistances for both the counter flow and parallel flow configurations are indistinguishable.
4. The counter flow arrangement provides better temperature uniformity for the entire flow rate range tested.
5. For both counter flow and parallel flows, total thermal resistance decreases as more fluid is pumped through the bottom microchannel layer. However, the pressure drop significantly increases.

Lei et al. [3] investigated the thermal and hydraulic performance of multilayer microchannel heat sinks experimentally. The structure of the test module is illustrated in Figure 5. The test module consists of a copper microchannel heat sink, a housing, a cover plate and a power intensifier. The housing and cover plate were made of a thermoplastic material with a thermal conductivity of 0.24 W/(m.°C). The geometry of the copper heat sinks is illustrated in Figure 6. The heat sinks were made of copper and the channels were precisely machined. Each heat sink was composed of several parts and the individual layers were soldered together. The dimensions of the copper heat sinks tested are presented in Table 2. All heat sink samples have same length and width - 1.2 × 0.5 inches (30.5 ×12.7 mm), channel dimensions of 0.02 × 0.02 inches (0.508 × 0.508 mm), base thickness of 0.02 inches (0.508 mm) and wall thickness of 0.04 inches (1.016 mm).

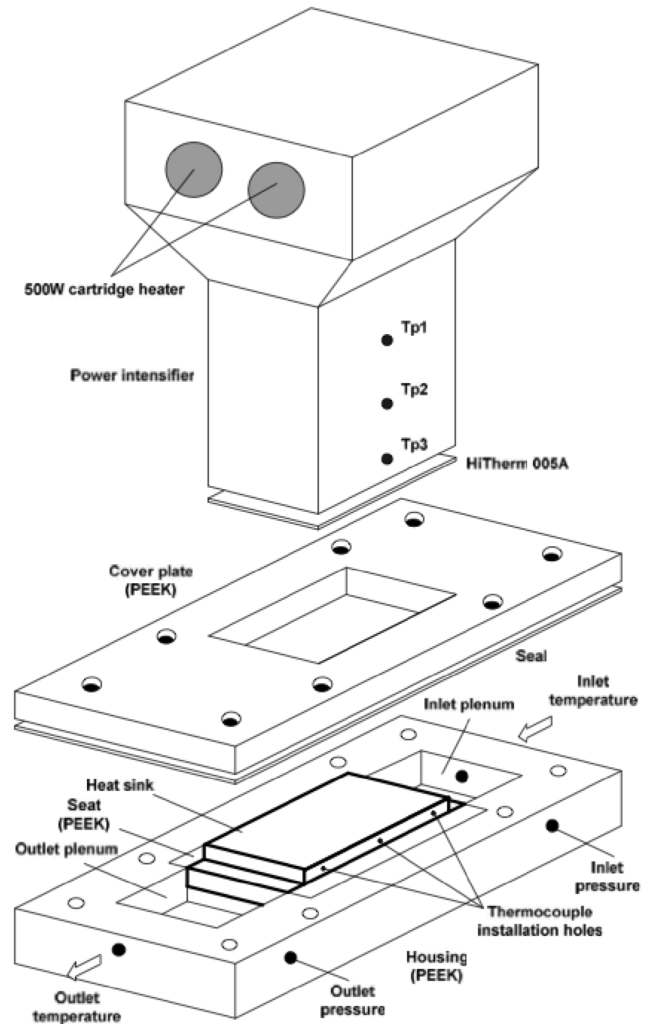

Figure 5. Test Module Configuration [3]

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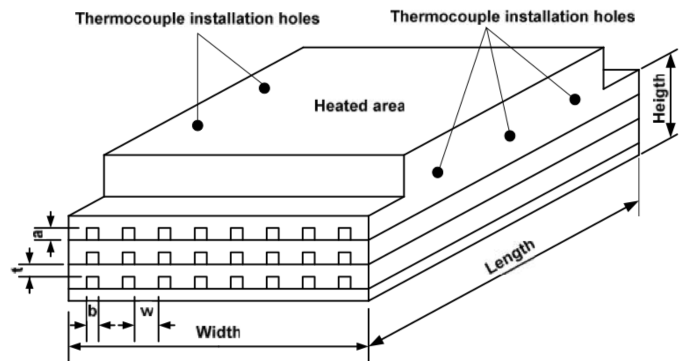

Figure 6. Copper Microchannel Heat Sink Geometry [3]

Sample ID	H (mm)	a×b (mm)	Channels/layer	No. of layers
Cu-1	1.52	0.508×0.508	8	1
Cu-2	2.54	0.508×0.508	8	2
Cu-3	3.56	0.508×0.508	8	3
Cu-4	4.57	0.508×0.508	8	4
Cu-5	5.59	0.508×0.508	8	5

Table 2. Copper Microchannel Heat Sink Dimensions [3]

Distilled water was used as the working fluid in the Lei's experiments. By comparing multilayer microchannel heat sinks with single-layer microchannel heat sinks, Lei et al. found that:

1. Multilayer microchannel heat sinks have smaller thermal resistance than single- layer heat sink at low water flow rate. For high flow rates, the flow inside single- layer heat sink becomes turbulent so it outperforms two-layer microchannel heat sinks, but 3, 4, and 5-layer heat sinks still outperform single-layer one due to much larger surface area.

2. At the same volumetric flow rates, multilayer microchannel heat sinks have a smaller pressure drop than single-layer ones due to their larger cross section areas, which lead to decreasing of flow velocity. For example, the 5-layer copper heat sink achieved a thermal resistance of 0.33 $K/W/cm^2$ with 0.03 Watts of pumping power in the experiments.

3. There is a limit on the maximum number of layers for practical purposes, since multilayer microchannel heat sinks have much larger volumes than single-layer microchannel heat sinks.

The studies of Wei [2] and Lei et al. [3] demonstrate the effectiveness of using stacked microchannel heat sinks to dissipate high heat fluxes. Compared to traditional single-layer microchannel heat sinks, stacked microchannel heat sinks have lower thermal resistance and require less pumping power. This means that the stacked microchannel heat sinks can keep the device temperature lower with less energy. As Wei [2] showed that the microchannel can be etched directly on a silicon die, it is feasible to integrate multilayer microchannel in 3D chips. However, making the multilayer microchannel is more difficult than a single-layer microchannel. There still are some application problems, such as sealing, flow distribution and fluid control that needed to be addressed before large scale usage can be attempted.

References:

1. http://www.zurich.ibm.com/news/10/moore.html.

2. Wei, X., Stacked Microchannel Heat Sinks for Liquid Cooling of Microelectronics Devices, Dissertation, Georgia Institute of Technology, November 2004.

3. Lei, N., Ortega, A., and Vaidyanathan, R., "Modeling and Optimization of Multilayer Minichannel Heat Sinks in Single-Phase Flow," Proceedings of the 2007 ASME International Electronics Packaging Conference (InterPACK 2007), Paper No. IPACK2007-33329, Vancouver, B.C., Canada, July 8-12, 2007.